AMENDMENTS TO THE CLAIMS

1. (*Canceled*)

2. (*Previously Presented*) A sensor as in claim 9, wherein said noise reduction circuit receives said amplified image signals and removes at least one amplifier offset therefrom.

3. (*Previously Presented*) A sensor as in claim 2 wherein said amplifier offset includes amplifier offsets from different rows of a column.

4. (*Previously Presented*) A sensor as in claim 2, further comprising an amplifier having said amplifier offset coupled between said plurality of image sensor pixels and said noise reduction circuit, wherein said amplifier includes an operational amplifier, a feedback capacitor connected across said operational amplifier, and a variable gain-setting capacitor at an input to said operational amplifier.

5-7. (*Canceled*)

8. (*Original*) A sensor as in claim 4, further comprising a reset transistor, coupled across said feedback capacitor, to reset a value of said feedback capacitor.

9. (*Currently Amended*) An image sensor comprising:

a plurality of image sensor pixels to provide a plurality of respective reset and signal voltages; and

a noise reduction circuit, said noise reduction circuit being adapted to receive a first amplified image signal formed of first reset and signal voltages and a second amplified image signal[[s]] formed of second reset and signal voltages, and being adapted to output a combination of said first and second amplified image signals at a first time, and said noise reduction circuit being adapted to receive a third amplified image signal formed of third reset and signal voltages and being adapted to output a combination of said second and third amplified image signals at a subsequent time;

wherein said noise reduction circuit includes a first fixed pattern noise reduction circuit, having a first capacitor element to store a difference between said first reset and signal voltages and a second capacitor ~~elements respectively storing~~ element to store a difference between said second ~~signal and~~ reset and signal voltages ~~amplified pixel values for said first amplified image signal~~, and a second fixed pattern noise reduction circuit, having a third capacitor element to store said difference between said second reset and signal voltages and a fourth ~~capacitors respectively storing~~ capacitor element to store a difference between said third reset and signal voltages; ~~and reset amplified pixel values for said second amplified image signal, and outputting combined signal and reset values for said first and second amplified image signals at said first time.~~

wherein said combination of said first and second amplified image signals includes a combination of said difference between said first reset and signal voltages and said difference between said second reset and signal voltages; and

wherein said combination of said second and third amplified image signals includes a combination of said difference between said second reset and signal voltages and said difference between said third reset and signal voltages.

10. (*Previously Presented*) A sensor as in claim 9, wherein said image sensor pixels are active pixels, each of which including a photoreceptor, and an in-pixel buffer transistor and an in-pixel selection transistor.

11. (*Canceled*)

12. (*Previously Presented*) A method as in claim 15 wherein n=2.

13-14. (*Canceled*)

15. (*Currently Amended*) A method of binning pixels, comprising:

first providing a plurality n of amplified pixel signals at a first time;

adding said n amplified pixel signals together to provide a first n-binned signal;

second providing another plurality n of amplified pixel signals at a second time, wherein said another plurality n of amplified pixel signals includes n-1 of the same amplified pixel signals as obtained in said first providing;

adding said another plurality n of amplified pixel signals to provide a second n-binned signal different from the first n-binned signal; and

using at least two separate noise reduction circuits, a first of which reduces noise in a first amplified pixel signal, a second of which reduces noise in a second amplified pixel signal, and said first and second amplified pixel signals being used to form said first n-binned signal, said second amplified pixel signal being retained for use with a third amplified pixel signal later processed by said first noise reduction circuit to form said second n-binned signal.

16. (*Canceled*)

17. (*Previously Presented*) A method as in claim 15, wherein said first providing comprises obtaining a chronologically first amplified pixel signal and subsequently obtaining a

chronologically second amplified pixel signal, and said adding to provide said first n-binned signal comprises adding said chronologically first and chronologically second amplified pixel signals.

18. (*Previously Presented*) A method as in claim 15, further comprising removing offsets from amplifiers that amplify said amplified pixel signals, prior to adding said pixel signals.

19. (*Currently Amended*) A binning sensor, comprising:

a plurality of pixels arranged in an array;

a configurable adder, selectively connected to add a plurality n of adjacent row pixel values to one another at a first time and then to add another plurality of said adjacent row pixel values to one another at a second time, wherein said plurality n of adjacent row pixel values and said another plurality of adjacent row pixel values have at least one common pixel value corresponding to a respective at least one common row element; and

an offset reduction circuit, removing certain amplifier offsets from said pixel values prior to said adding;

wherein said offset reduction circuit is operable to store first pixel values of said plurality n of adjacent row pixel values not corresponding to said at least one common row element on first capacitor elements for use at the first time, to subsequently store second pixel values of said another plurality of said adjacent row pixel values not corresponding to said at least one common row element on said first capacitor elements for use at the second time, and to store third pixel values corresponding to said at least one common row element on second capacitor elements for use at the first time and the second time.

20. (*Previously Presented*) A sensor as in claim 19, wherein the number of pixels added equals n and said offset reduction circuit includes n noise reduction circuit parts.

21-23. (*Canceled*)

24. (*Currently Amended*) A sensor as in claim 9, wherein said first fixed pattern noise reduction circuit is operable to store said third reset and signal ~~and reset values for said third image part~~ voltages on said first ~~and second~~ capacitor[[s]] element~~, said noise reduction circuit being operable to output combined signal and reset values for said second image part and said third image part,~~ to thereby re-use said third reset and signal ~~and reset values for said second image part~~ voltages at two different times.

25. (*Previously Presented*) A method as in claim 17, wherein said second providing comprises obtaining a chronologically third amplified pixel signal, and wherein said adding to provide said second n-binned signal comprises adding said chronologically second and chronologically third amplified pixel signals.

26. (*Previously Presented*) A method as in claim 15 wherein n=2.

27. (*Previously Presented*) An image sensor comprising:

a plurality of image sensor pixels, including first, second, third, and fourth pixels to provide respective first, second, third, and fourth pixel signals; and

a noise reduction circuit to provide a first combined pixel signal at a first time based on said first and second pixel signals, a second combined pixel signal at a second time based on said second and third pixel signals, and a third combined pixel signal at a third time based on said third and fourth pixel signals; and

a plurality of capacitor elements, including first, second, third, and fourth capacitor elements, wherein said first and second capacitor elements store respective said first and second pixel signals for said first combined pixel signal, wherein said third and fourth capacitor elements

store respective said second and third pixel signals for said second combined pixel signal, and wherein said first and second capacitor elements store respective said third and fourth pixel signals for said third combined pixel signal.

28. (*Previously Presented*) An image sensor as in claim 27, further comprising:

an amplifier to amplify said first, second, third, and fourth pixel signals, said amplifier including:

an operational amplifier having an inverting input terminal, a non-inverting input terminal, and an output terminal;

a feedback capacitor coupled between said output terminal and said inverting input terminal; and

a variable gain-setting capacitor coupled to said inverting input terminal.

29. (*Previously Presented*) An image sensor as in claim 28, wherein said noise reduction circuit is configured to remove at least one amplifier offset of said amplifier.

30. (*Previously Presented*) An image sensor as in claim 27, wherein said first, second, third, and fourth pixels are active pixels, each including a photoreceptor, an in-pixel buffer transistor, and an in-pixel selection transistor.

31. (*New*) An image sensor comprising:

a plurality of image sensor pixels including at least first, second, and third pixels to provide respective sets of first, second, and third reset and signal voltages; and

a noise reduction circuit to receive first, second, and third amplified image signals formed of differences between the reset and signal voltages of the respective first, second, and third sets, the noise reduction circuit including

a first fixed pattern noise reduction circuit having

a first capacitor element to store the first amplified image signal,

a second capacitor element to store the second amplified image signal, and

circuitry configured to combine the first and second amplified signals to provide a first combined signal at a first time; and

a second fixed pattern noise reduction circuit having

a third capacitor element to store the second amplified image signal,

a fourth capacitor element to store the third amplified image signal, and

circuitry configured to combine the second and third amplified signals to provide a second combined signal at a second time that is different from the first time.